This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

What is claimed is:

1. (previously amended) A processor comprising:

at least one local storage designed to contain a plurality of floating point values;

at least one floating point execution unit, said floating point execution unit further including a separator configured to retrieve said plurality of floating point values from said local storage and make available a mantissa portion from and corresponding to each of said plurality of floating point values, said floating point execution unit further including at least one adder unit configured to receive said mantissas in an order and number determined by said adder unit;

a compare unit operatively coupled to said at least one local storage further comprising a separator configured to retrieve said plurality of floating point values from said local storage and make available at least a mantissa portion of each of said floating point values, and the compare unit configured to make available a carry-out bit value resulting from an addition of said mantissas portions;

an end-around-carry bit calculator unit operatively coupled to said compare unit and configured to provide a correct value of an end-around-carry calculation available as output, based on values received from said compare unit ; and

a rounding calculator operatively coupled to the end-around-carry bit calculator to calculate a rounding choice upon having the adder unit complete the addition and communicating the choice to the adder unit.

2. (original) The processor of claim 1 where said compare unit further comprises as a component contained therein said end-around-carry bit calculator unit.

3. (original) The processor of claim 1 where said at least one floating point execution unit further comprises as a component therein said end-around-carry bit calculator unit.

4. (currently amended) A machine readable medium containing a data structure having an instruction therein for determining which values from a local storage containing floating point values to send to a floating point execution unit, and in parallel to a compare unit, where said compare unit and said floating point execution unit are operatively coupled to an end-around-carry value calculator and a rounding calculator that is operatively coupled to the end-around-carry value calculator, the rounding calculator calculates a rounding choice contemporaneously as an adder unit performs an addition ~~to~~ and provide the rounding choice to ~~an~~ the adder unit ~~upon having~~ at the instant the adder unit complete the addition.

5. (currently amended) A method for providing a correct rounding choice for floating point subtraction comprising:

(a) providing a first floating point value having a sign, an exponent, and a mantissa;

(b) providing a second floating point value having a second sign, a second exponent, and a second mantissa;

(c) performing a compare of said two floating point values while starting a subtraction of said first and second mantissas in an adder unit;

(d) calculating an end-around-carry value using results from said compare;

(e) using said end-around-carry value to calculate the rounding choice contemporaneously as the adder unit performs the subtraction; and

(f) providing said rounding choice to an adder unit ~~upon having~~ at the instant the adder unit complete said subtraction.

6. (currently amended) A method for providing increased parallelism in a processor comprising:

(a) providing a first floating point value having a sign, an exponent, and a mantissa;

(b) providing a second floating point value having a second sign, a second exponent, and a second mantissa;

(c) starting in parallel a compare of said first and second floating point values, and an addition of said first and second floating point values in an adder unit, where said addition is using the 2's compliment form of said second mantissa;

(d) using said compare results to calculate an end-around-carry value;

(e) calculating a rounding choice using the end-around-carry value contemporaneously as the adder unit performs the addition ; and

(e) providing the rounding choice to ~~an~~ the adder unit ~~upon having~~ at the instant the adder unit completes said addition.

7. (previously amended) A method for computing a floating point subtraction comprising:

(a) providing a first floating point value having a sign, an exponent, and a mantissa;

(b) providing a second floating point value having a second sign, a second exponent, and a second mantissa;

(c) performing a compare of said two floating point values and providing the output of said compare to an end-around-carry calculator unit;

(d) calculating an end-around-carry value in said end-around-carry calculator unit;

(e) sending said first and second mantissas to an adder;

(f) aligning said second mantissa to said first mantissa in said adder;

(g) starting an addition of said first mantissa and a two's compliment form of said second mantissa in said adder;

(h) providing said calculated end-around-carry value;

(i) using said end-around-carry value to calculate a Guard Round Sticky and determine a rounding choice before said addition is completed;

(j) completing said addition in said adder;

(k) using said rounding choice to choose a correct rounded answer from said addition upon having said addition is completed; and

(l) providing a final answer using said rounding choice, said first and second signs, and said first and second exponents;